

substrate comprising the steps of:

(a) providing a pad stack atop a surface of a substrate having regions for forming apertures therein, said pad stack including at least a top patterned masking layer that exposes portions of said pad stack, said top patterned masking layer serving as the single critical mask used in defining apertures in said substrate;

(b) blocking at least one of said regions of said substrate with a first block mask, while leaving at least one other region of said substrate unblocked;

(c) forming a plurality of first apertures having a first depth in said unblocked region of said substrate using said patterned masking layer to define said plurality of first apertures by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate, said first apertures having sidewalls that are aligned to outer edges of the top patterned masking layer;

(d) removing said first block mask; and

(e) forming a plurality of second apertures having a second depth in regions of said substrate that were previously blocked by said first block mask using said patterned masking layer to define said second apertures, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second apertures having sidewalls that are aligned to outer edges of the top patterned masking layer which are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.

12. (Amended) A method of forming multi-depth isolation regions in a semiconductor substrate comprising the steps of:

(a) providing a pad stack atop a surface of a semiconductor substrate having regions for forming trench isolation regions therein, said pad stack including at least a top patterned masking layer that exposes portions of said pad stack, said top patterned masking layer serving as the single critical mask used in defining trenches in

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said substrate;

(b) blocking at least one of said regions of said semiconductor substrate with a first block mask, while leaving at least one other region of said semiconductor substrate unblocked;

(c) forming a plurality of first trench isolation regions having a first depth in said unblocked region of said semiconductor substrate using said patterned masking layer to define said plurality of first trench isolation regions by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate, said first trench isolation regions having sidewalls that are aligned to outer edges of the top patterned masking layer;

(d) removing said first block mask; and

(e) forming a plurality of second trench isolation regions having a second depth in regions of said semiconductor substrate that were previously blocked by said first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions having sidewalls that